Asymmetrical DC-DC Converter with Fault Tolerant Operation Capability for Distributed Generation

Zhengzhao He¹, Wenping Cao¹, Zhengyu Lin¹ and Yihua Hu²

1. School of Engineering and Applied Science, Aston University, Birmingham B4 7ET, United Kingdom
2. School of Electrical Engineering & Electronics, University of Liverpool, Liverpool L69 3BX, United Kingdom

Corresponding author: Wenping Cao (w.p.cao@aston.ac.uk)

Abstract: As the costs of manufacturing photovoltaic (PV) panels continue to decrease, the use of PV-based solar energy systems is seen in rise across the globe. This paper proposes an asymmetrical DC-DC converter for standalone solar energy systems. The converter is developed to control modularized PV panels with a combination of soft-switching, flyback-forward, high-step-up voltage ratio, and fault tolerant operation features. This topology can achieve maximum power point tracking (MPPT) control while delivering a high voltage gain and an efficiency of 92-95% over a wide range of outputs by phase shift control. The entire system is firstly simulated and refined using the PSIM software and tested experimentally on a 300 W prototype. The key feature is its fault tolerant operation capability without the use of extra fault diagnosis circuitry. The proposed technique can be applied to grid-tied solar energy systems and fuel-cell DC systems.

Keywords: Asymmetrical converter, fault tolerance, DC-DC converter, MPPT, photovoltaic power.

Nomenclature

S₁, S₂ | Main switching
L₁, L₂ | Coupled inductor
S₁, S₂ | Auxiliary reverse-connected switches
C₁, C₂ | Voltage double capacitor
C₁, C₂ | Clamping capacitors
C₁, C₂ | Parallel capacitors the main switches
L₁a, L₂a | Primary winding
L₁b, L₂b | Secondary winding
L₁L₁, L₂L₂ | Leakage inductance
C₁, C₂ | Output capacitor
D₁, D₂, D₃, D₄ | Output diode
V₀ | Input voltage
V₀ | Output voltage
│ | Load
N | Turns ratio

1. Introduction

Environmental issues have been a major concern for decades thus leading to the increased development of renewable energy technologies. Solar energy is one major source of green energy, which has been utilized in electric systems since 1880s and is being utilized in large quantity economically nowadays. According to an International Renewable Energy Agency report and BP Statistical Review of World Energy 2016 [1], from 2000 to 2015, the capacity of global photovoltaic power increased from 1,313 to 230,606 MW and the power generated increased from 1,090 to 253,037 GWh. The research indicates a dramatic increase in solar power within these 15 years, as shown in Fig. 1.

Commercial PV panels have a relatively low DC voltage output (15-20 V) while the local grid is AC at 230V. In reality, in order to connect PV panels to the grid, a DC converter is necessary to boost the voltage level before inverting the DC voltage into AC voltage. According to Ref. [2], there are three types of grid-connected DC converters for PV systems. Their configurations are demonstrated in Fig. 2. In this figure,
the central type has only one DC converter for the entire PV system, all the PV panels have been connected as a matrix. Panels have been divided into groups: they are series connected within each group to increase the output voltage; and those groups are then parallel connected to increase the output current. In order to gain maximum power output for the entire system, the control algorithm of the DC converter could be complicated and even with the best solution, each individual PV panel is compromised by the other for different surrounding environment. This configuration applies in high voltage and high power PV system, with the capability of large current output. However, it would cause high power loss for the reasons discussed above. The string type grid-connected DC converter uses DC converter to stabilize the output voltage for only series connected PV panels. It would have better output performance than the first one, although, not all the PV panels can work under maximum power output. The DC converters, used in string type, have lower rated output power. In modularized type, every PV panel has individual DC converter to boost the voltage to grid level. In this configuration, all the panel can work under maximum power output condition, because each panel is controlled under individual DC converter. However, the voltage gain of these DC converters is extremely high [3, 4]. In practical situation, the third configuration is the most widely applied one and is therefore the focus of this paper.

For DC converters, there are two issues to be considered when dealing with high voltage gain. The first difficulty is extreme duty cycle. Duty cycle of the main switch has major influence on the voltage gain. High voltage gain in conventional DC topology would lead to extreme low or high duty cycle. In this situation, current ripple would be an obstacle regarding output quality. High turns ratio in isolated DC converters would be the second issue. High turns ratio would lead to high leakage inductance, with the consequence of reduced voltage gain and energy losses.

In theory, the output voltage of one PV string is low and varies over a wide range in case of the change of weather or even the shadow effect despite the use of MPPT. On one hand, this requires the front-end DC-DC converter to be equipped with a high step-up capability for grid connection. On the other hand, the multilevel converters are capable to deliver outstanding output waveforms, reduce filter sizes and reduced electromagnetic interference (EMI).

However, the drawbacks of these converters are their high complexity, high price and low voltage...
amplification. Now, it is a task to develop a new topology that combined high-step-up and minimal number of switching devices for grid-connected PV systems [5-7].

For the requirement of voltage gain which is very high when applied to each PV cell, two issues require attention when using conventional DC converters [8]. Firstly, Extreme duty cycle would generate high current ripple, and makes the system more complicated to control and monitor. Secondly, high voltage stress on the power devices would increase the conduct losses and requires better device performance.

Introducing high frequency transformer into the circuit is another answer to high voltage gain and it is widely employed. It avoids the extreme duty cycle by simply introducing turns ratio N between the primary end and secondary end of the transformer into the equation [9-12]. Multiple topologies with transformer are being brought up in recent years, with or without electric isolation. The combination of different concepts enhances the capability of the converter. From Fig. 3, the high-step-up converter employs multilevel structure and flyback-forward structure, which dramatically reduces the harmonic distortion and increases system stability when output demand varies.

Voltage multiple cell, indicated in Fig. 4 is also very common in DC converter; using additional capacitor and diode, the output voltage could be doubled without any major alteration to the circuit. All the techniques mentioned above could all achieve high voltage gain. However, large current ripple becomes inevitable, since input current rises. It also, in turn, leads to higher device current withstand level and increases the conduct losses. Interleaved structure is an effective way to solve the problem, by proper phase shift control. The current ripple could be significantly reduced and the withstand current level of power device can be lowered [9, 14-16]. However, it would double the number of components and increase the control complexity.

This paper proposes a new asymmetry DC-DC converter which consists of interleaved inductors, clamping capacitors, coupled inductors and voltage quadruple cell unit. The equivalent circuit of the proposed converter is shown in Fig. 5.

2. System Structure and Analysis

Based on the above topologies, the proposed converter is analyzed in detail as follows.

2.1 Circuit Configuration and Description

In Fig. 5, the two main switching legs are constituted by $S_1$ and $S_2$, $L_1$ and $L_2$. $S_1$ and $S_2$ are the main switches connected in parallel to achieve interleaved structure for coupled $L_1$ and $L_2$, which can reduce the volume of the inductance for certain input current ripple requirement. These coupled inductors have primary turns of $N_1$. The auxiliary reverse-connected switches $S_{c1}$, $S_{c2}$ and the clamping
capacitors $C_{c1}$ and $C_{c2}$ comprise the active-clamping circuit for those two main switching legs; which recycle the leakage energy caused by leakage inductance, and realizes zero voltage switching (ZVS) for the primary power devices. The parallel capacitors $C_{s1}$ and $C_{s2}$ of the main switches are also used to implement ZVS.

2.2 Operational Analysis

Two signals with the same frequency and duty cycle are applied to the main switches $S_1$ and $S_2$, as shown in Fig. 6. Due to the asymmetrical connection, the signal of $S_1$ leads the other by 160°, while the auxiliary switches are complementary with their corresponding main switches. Using steady state analysis, 15 stages can be classified. The stages are illustrated in Fig. 7 and described as follow:

Stage 1 [$t_0$−$t_1$]: During this stage, both of the main switches $S_1$ and $S_2$ are in the turn-on state. The clamp switches $S_{c1}$ and $S_{c2}$ are in the turn-off state. And the output diodes $D_{o1}$ and $D_{o2}$ are both reverse-biased. The two coupled inductors operate in the flyback mode to store the energy. The primary winding currents $I_{1a}$, $I_{2a}$ are stable which generate no current at the secondary inductor. The energy to the load is provided by the secondary output capacitors $C_{o1}$ and $C_{o2}$.

Stage 2 [$t_1$−$t_2$]: One of the main switches $S_1$ turns off at the beginning of this stage, it results in a nearly linear increase of the main switches, combining the existence of the parallel capacitor $C_{s1}$. This interval is very short because the primary winding current is large and the parallel capacitor is small.

Stage 3 [$t_2$−$t_3$]: The drain-source voltage keeps increasing until $t_3$, drain-source voltage is larger than the voltage of clamp capacitor $C_{c1}$ which makes the parallel-reversed diode of clamp switch conduct. The voltage of the clamp capacitor begins to increase for the charging of primary winding current $I_{1a}$. From this stage, the $C_{c1}$ and $L_{1a}$ begin to resonate.

Stage 4 [$t_3$−$t_4$]: Due to the positive direction of the diode, the voltage across the clamp switch $S_{c1}$ falls to zero at $t_3$. The turn-on signal is applied to the switch at the same time, which achieves ZVS turn-on operation. The current then transfers from the diode to the switch quickly. The increase of the voltage of $C_1$ leads to decrease of the primary winding current $I_{1a}$, which causes the increase of the voltage on the secondary winding and the generation of the current $I_{1b}$. However, due to diode $D_{o3}$ and $D_{o4}$, the secondary winding current $I_{2a}$ can only flow within the following path $L_{1a}$-$C_{1}$-$D_{o4}$-$L_{2a}$-$L_{1b}$, namely Path 1. In this stage, $L_1$ operates at forward mode and $L_2$ stays at backward mode for the reverse direction increase of $I_{2b}$, which leads to the increase of $I_{2a}$.

Stage 5 [$t_4$−$t_5$]: The primary winding current $I_{1a}$ falls to zero at $t_4$, because of the resonation, $I_{1a}$ keeps dropping, which means, the capacitor also begins to discharge at the beginning of this stage.

Stage 6 [$t_5$−$t_6$]: At $t_5$, the turn-off signal is applied to the clamp switch $S_{c1}$, this is a ZVS turn-off operation condition because of $C_{s1}$. It restricts the increasing rate of the drain-source voltage of main switch $S_1$, making it a nearly linear growth. The primary winding current $I_{1a}$ begin to increase, which leads to the decrease of the secondary winding current $I_{1b}$. However, due to the existence of $L_{2b}$, the current through $L_{2b}$ cannot decrease as fast as $I_{1b}$, and then two new current paths appear. Apart from path 1, the other two paths are: Path 2 ($L_{2a}$-$C_{2}$-$D_{o1}$-$C_{o1}$-$L_{2b}$) and Path 3 ($L_{2a}$-$C_{2}$-$D_{o1}$-$R$-$C_{o2}$-$L_{2b}$). And it is obvious that, Path 2 is charging $C_{o1}$, while Path 3 is discharging $C_{o2}$. The
Asymmetrical DC-DC Converter with Fault Tolerant Operation Capability for Distributed Generation
L_{2b} begins to operate at forward mode. The primary winding current of L_{2b} starts to fall. One part of the leakage energy is delivering to the secondary winding L_{2b}, C_{o1} and R, while another part is recycled to the input source.

Stage 7 \([t_5-t_6]\): At t_6, the primary winding current \(I_{1a}\) return to stable state, the inductor \(L_{1a}\) operates at flyback-mode to store energy again. For the stability of \(I_{1a}\), the secondary winding current \(I_{1b}\) falls to zero. Then, the current paths have only Path 2 and Path 3 left. Without the source, the current of both paths continue to drop.

Stage 8 \([t_7-t_8]\): At the beginning of this stage, the currents in Path 2 and Path 3 fall to zero. The rest part of this stage is the same with stage 1.

Stage 9 \([t_8-t_9]\): The turn-off signal applied to the main switch S_2. It is still the same with stage 2.

Stage 10 \([t_9-t_{10}]\): This stage is similar to stage 3.

Stage 11 \([t_{10}-t_{11}]\): The primary end has the similar operation as stage 4. And, due to the reverse direction increase of \(I_{1b}\), the corresponding primary winding current \(I_{1a}\) begin to increase, similar to the behaviour of \(I_{1b}\) in stage 3. However, for the secondary end which differed from stage 3, the secondary winding current spilt up to three different paths: Path 4 \((L_{2b}C_2-L_{2b})\), Path 5 \((L_{2b}C_{o1}R-D_03C_{1}L_{1b})\) and Path 6 \((L_{2b}C_{o2}D_03C_{1}L_{1b})\). Moreover, the power for the load in this stage is provided by \(C_{o1}\) and the energy from the source, while the other output capacitor \(C_{o2}\) is charging.

Stage 12 \([t_{11}-t_{12}]\): Similar to stage 5.

Stage 13 \([t_{12}-t_{13}]\): The primary end of this stage share similarity with stage 7. The increase of \(I_{2a}\) leads to decrease of \(I_{2b}\). Because the current flow through \(C_2\) is only affected by \(L_{2b}\), the decrease rate of \(I_{2b}\) is fast; while the current flow through Path 5 and Path 6 decrease much slower than Path 4 for the existence of \(L_{1b}\).

Stage 14 \([t_{13}-t_{14}]\): At the beginning of this stage, the current of Path 4 falls to zero. The amplitudes of \(I_{2b}\) and \(I_{2a}\) are identical and both continue dropping, which leads to change of primary winding current value.

Stage 15 \([t_{14}-t_{15}]\): At \(t_{15}\), the residual current of the secondary winding falls to zero. The rest part is similar to stage 1.

3. Steady-State Circuit Performance Analysis

To simplify the analytical procedure, the following assumptions are made

- The two couple inductors \(L_1\) and \(L_2\) are identical;
- The two clamping capacitors \(C_{s1}\) and \(C_{s2}\) are identical;
- The two voltage double cell capacitors \(C_1\) and \(C_2\) are identical;
- The voltages of all capacitors are constant;
- Neglecting the dead time effect;
- Neglecting voltage drop of all diodes and internal resistance of all devices.

These assumptions can be expressed as

\[
L_{m1} = L_{m2} = L_m \quad (1) \\
L_{Lk1} = L_{Lk2} = L_{Lk} \quad (2) \\
C_{c1} = C_{c2} = C_c \quad (3) \\
C_1 = C_2 = C \quad (4)
\]
3.1 Voltage Gain Derivation

The charging process of the first leg switching period can be calculated by \( I_c \) during \( t_5 \) and \( t_7 \). And for the second leg the process can be obtained by \( I_{L1b} \) during \( t_{10} \) and \( t_{14} \). The charge of the load within a period can be derived as

\[
Q_{\text{load}} = Q_{co1} + Q_{co2} = Q_c1 + Q_c2 \quad (5)
\]

where \( Q_{co1} \) and \( Q_{co2} \) are the charges that go through \( C_{o1} \) and \( C_{o2} \), and \( Q_c1 \) and \( Q_c2 \) are for \( C_1 \) and \( C_2 \). \( Q_c1 \) equals to the integration of the current flows out of the capacitor \( C_1 \), which means the area of \( I_c \) within \([t_5~t_7]\). By the same principle, \( Q_c2 \) equals to the area of \( IL_{1b} \) within \([t_{10}~t_{14}]\). However, due to charging balance of the voltage double capacitors and the fact that \( C_2 \) is only charged and discharged by \( I_c \), \( C_1 \) is only affected by \( IL_{1b} \). These two currents can be transferred to \( I_c \) during \([t_{10}, t_{13}] \) \( IL_{1b} \) during \([t_3, t_6] \), respectively. Then Eq. (5) can be expressed as

\[
Q_{\text{load}} = A_{1l1b,3~6} + A_{ILc,10~13} \quad (6)
\]

Then the voltage gain of the output can be expressed as follow:

\[
M_{lk} = \sqrt{\frac{N(1-D)RT_e}{L_{lk}}} \left( \frac{1}{1-D} \right) + B \left( \frac{2}{1-D} \right) A_{RT_e} \frac{N^2(1-D)RT_e}{L_{lk}} \left( \frac{1}{1-D} \right) \quad (7)
\]

If assumed the \( L_{lk} \) to be very small for the proposed converter, then the gain expression can be simplified as

\[
M_{\text{simp}} = \sqrt{\frac{N(1-D)RT_e}{L_{lk}}} \left( \frac{2}{N^2} \right) A_{RT_e} \frac{N(1-D)RT_e}{L_{lk}} \left( \frac{1}{1-D} \right) \quad (8)
\]

From the above equations, it can be concluded that the voltage gain of the proposed converter is determined by the turns ratio of the coupled inductors, the duty ratio of the main switches, the leakage inductance, the switching frequency and the output load.

3.2 Voltage Stress Analysis

The voltage stress for the main switches is the voltage of clamping capacitors:

\[
V_{\text{ds, stress}} = V_{cc} = \frac{V_{\text{in}}}{1-D} \approx \frac{V_{\text{out}}}{2N} \quad (9)
\]

The maximum voltage stress of \( D_{o1}, D_{o2}, D_{o3} \) and \( D_{o4} \) are

\[
\begin{align*}
V_{Do1} &= \frac{2}{3}V_{\text{out}} \quad (10) \\
V_{Do2} &= \frac{1}{6}V_{\text{out}} \quad (11) \\
V_{Do3} &= \frac{5}{6}V_{\text{out}} \quad (12) \\
V_{Do4} &= \frac{5}{6}V_{\text{out}} \quad (13)
\end{align*}
\]

It is obvious that to achieve certain amount of voltage gain, the switching devices should be selected by considering the turns ratio of the coupled inductors and the resulting voltage stress.

4. Simulation Result and Analysis

A specific case study of the proposed DC-DC converter has been carried out. Using PSIM software program, the converter was designed using certain parameters.

4.1 System Set Up

An asymmetric isolated DC-DC converter was built using PSIM software. Fig. 8 indicates the configuration of the proposed converter.

In this case, a single PV panel is connected as an input source of the proposed converter, which has current and power limitation. For the purpose of topology testing, all the components are ideal except the transformers, whose magnetizing inductance and leakage inductance are still taken into consideration. To simplify the circuit, the auxiliary capacitors parallel-connected to the auxiliary switches are eliminated; the system is operated at a very high carrier frequency, and the two switches are not affecting each other.
The system parameter is shown in Table 1 and maximum power output of PV 156.1 W at 17.1 V. In order to present clear waveforms for analysis during each switching period, the switching angle between the two main control legs is 165 degrees.

4.2 MPPT Simulation

The proposed DC converter was tested under basic MPPT module based on PSIM software. The following table above shows the parameters of the MPPT converter. The light intensity input is given by square waveform from 70-100% of its standard value and switching frequency was set to 10 Hz. For residential and commercial PV system, there are usually 20-30 PV panels with rated power of 150 W for each PV panel. The performance of the actual system with even distribution structure can be better than the simulated three PV system.

4.3 Fault Tolerance and Operation

In this paper, only main switch open circuit faults are simulated and analyzed. The primary end is interleaved structure, and this topology allows the entire system to operate in two stages individually. The converter itself would still operate with one open circuit fault. However, the secondary ends of the transformers are asymmetrical connected.

4.4 Simulation Results

The configured converter was simulated based on 50 kHz carrier shown and the phase shift comparison of the converter output in Figs. 9 and 10, respectively. And time sampling time step is set to 0.2 µs.

From the result, it clearly indicates that the proposed converter is working properly, and the resulting waveform is very close to the theoretically deduced waveform presented in Fig. 6.

Figs. 11-12 show the simulation result of the MPPT. The unmatched parts of maximum PV output and actual output is caused by unbalanced input power and

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clamping capacitor (µF)</td>
<td>100</td>
</tr>
<tr>
<td>Transformer turns ratio</td>
<td>1:2</td>
</tr>
<tr>
<td>Transformer magnetizing inductance (µH)</td>
<td>50</td>
</tr>
<tr>
<td>Transformer leakage inductance (pri) (µH)</td>
<td>0.8</td>
</tr>
<tr>
<td>Transformer leakage inductance (sec) (µH)</td>
<td>0.2</td>
</tr>
<tr>
<td>Voltage doubler capacitance (µF)</td>
<td>4.2</td>
</tr>
<tr>
<td>Output capacitance(each) (µF)</td>
<td>100</td>
</tr>
<tr>
<td>Load battery voltage (V)</td>
<td>380</td>
</tr>
</tbody>
</table>

Fig. 9  Simulation result from PSIM software with 50 kHz carrier waveform [0.3, 0.30005] s: (a) carrier waveform; (b) current waveform $I_a$, $I_b$ of the primary side; (c) current waveform $I_a$, $I_b$, $I_c$ of the secondary side; (d) Current waveform of four output diodes; (e) output current.
Asymmetrical DC-DC Converter with Fault Tolerant Operation Capability for Distributed Generation

Fig. 10 Converter output: (a) output current waveform compared with current waveform through output diode $D_1$ and $D_3$ in three-interleaved topology (non-phase-shift); (b) output current waveform compared with current waveform through output diode $D_1$ and $D_3$ in three-interleaved topology (phase-shift).

Fig. 11 Main switch open circuit fault transit: (a) $G_a$ fault; (b) $G_b$ fault.

Output power of the entire system.

Under the assumption of ideal circumstance, no energy consuming element was included in this simulated system. However, with the existence of leakage inductance in transformer, the power dissipates into the air. From Eq. (22), the leakage inductance, load resistance and carrier frequency would affect the voltage gain, which in turn, affects the efficiency. Fig. 12a indicates that the efficiency drops with the decrease of carrier frequency; meanwhile, the high frequency brings more stability to the system, which can be told by the input and output current ripple.

Phase-shift technique is quite an important control scheme for interleaved structure like what is proposed in this paper. With properly tuning PI control, the converter could achieve better output flexibility when small variation occurs without major tuning of the duty ratio of the switches. In Fig. 12b, the simulation result indicates that voltage gain can be controlled by phase-shift method while maintaining high efficiency and duty ratio; however, the relationship is highly non-linear, it would be hard to achieve accurate control.

5. Experimental Results

The proposed topology is tested with a DC power supply as input source, an eZdsp 28335 to generate the PWM waveform, and an 800Ω resistive load for energy consumption. The IGBT is driven by MCP1406E MOSFET/IGBT driver fed by A3120 opt-coupler; the entire drive system is powered by
TJ-IB2415LS DC-DC converter. The circuit is tested under open circuit PWM control with fix duty cycle varying from 0.2 to 0.55, switching frequency changes from 10 to 30 kHz, and input voltage tuning from 5 to 30 V. Figs. 13-17 indicate experiment results regarding the relationship between gain ratio and input voltage (and switching frequency, duty ratio); efficiency and input voltage (and switching frequency, duty ratio). Due to the fixed duty ratio, and load resistance, increasing the input voltage means increasing the power flow through the converter. Because there are fixed power losses in practical systems, the system efficiency and the voltage gain would increase when the input power increases. Figs. 18 and 19 show soft-switching performance is achieved for overlap turn-on and non-overlap turn-on of the two major switches; the high-lighted circles in these two pictures are the interval of soft-switching.

Fig. 13  Voltage gain vs. $V_{in}$.

Fig. 14  Efficiency vs. $V_{in}$.

Fig. 15  Voltage gain vs. switching frequency.

Fig. 16  Voltage gain vs. duty ratio.

Fig. 17  Efficiency vs. duty ratio.

Fig. 18  Main switch current indicating soft-switching for $D = 0.4$.

Fig. 19  Main switch current indicating soft-switching for $D = 0.55$. 
6. Conclusions

This paper has presented a flyback-forward asymmetrical DC-DC converter with active clamping circuit. It employs the voltage multipliers and transformers. Flyback-forward structure combines the attractive feature of standalone flyback and forward topologies. The interleaved connection at the primary end of transformer reduces the current stress of the active component; and active-clamp circuits achieve ZCS turn-off, which increases the efficiency of the converter. The simulation results indicate that the topology could be applied to PV-to-grid systems. The fault tolerant capability is also validated in simulation. Experimental results confirm its effectiveness of the proposed topology. Compared to the symmetrical DC-DC converters, the proposed topology can achieve a higher voltage gain and a higher efficiency.

References


